AMENDMENTS TO THE SPECIFICATION

Kindly replace the Title of the Invention with the following amended title:

Method and apparatus for multiple byte or page mode programming ~~and reading~~ of a flash memory array

Kindly replace paragraph [0017] with the following amended paragraph:

[0017] These and other disadvantages are overcome individually or collectively in various embodiments of the present invention. For example, one embodiment of the present invention is a memory having a memory array that is programmed using negative substrate bias, and further having a voltage source for placing a negative bias on control gates of unselected memory cells subject to program-disturb to reduce the effect. ~~Another embodiment of the present invention is a memory having a memory array that is programmed using negative substrate bias, and further having a voltage source for~~ placing ~~a negative bias on control gates of unselected memory cells subject to read-disturb to reduce the effect.~~

Kindly add the following new paragraphs after paragraph [0018]:

[0018.1] Yet another embodiment of the present invention is a NOR-type memory integrated circuit comprising a plurality of word select lines; a plurality of bit lines; a plurality of source lines; a memory array having a plurality of adjustable threshold voltage memory transistors, each being programmable using channel-initiated secondary electron injection and having a source coupled to one of the source lines, a drain coupled to one of the bit lines, a floating gate overlying a channel defined in a substrate body region between the source and the drain, and a control gate overlying the floating gate and coupled to one of the word select lines; a voltage source for applying a body voltage to the substrate body regions containing the channels; a voltage source for applying a source voltage to the sources of at least a first and a second of the memory transistors via a common one of the source lines; a voltage source for applying a drain programming voltage to the drains of the first and second memory transistors via a common one of the column lines, the source and drain programming voltages being sufficient to generate channel-initiated secondary hot electrons in the respective channels of the first and second

memory transistors; a voltage source for applying a select voltage to the gate of the first memory transistor via a first one of the word select lines, the select voltage having a polarity and magnitude relative to the body voltage sufficient to attract the hot electrons of the first memory transistor and change the threshold voltage thereof to a programmed state; and a voltage source for applying an unselect voltage to the gate of the second memory cell via a second one of the word select lines, the unselect voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons of the second memory transistor and deter change in the threshold voltage thereof.

[0018.2] Yet another embodiment of the present invention is a virtual ground-type memory integrated circuit comprising a plurality of word select lines; a plurality of column lines; a memory array having a plurality of adjustable threshold voltage memory transistors, each being programmable using channel-initiated secondary electron injection and having a source coupled to one of the column lines, a drain coupled to an adjacent one of the column lines, a floating gate overlying a channel defined in a substrate body region between the source and the drain, and a control gate overlying the floating gate and coupled to one of the word select lines; a voltage source for applying a body voltage to the substrate body regions containing the channels; a voltage source for applying a reference voltage to the sources of at least a first and a second of the memory transistors via a first one of the column lines; a voltage source for applying a programming voltage to the drains of the first and second memory transistors via a second one of the column lines adjacent the first column line, the reference and programming voltages being sufficient to generate channel-initiated secondary hot electrons in the respective channels of the first and second memory transistors; a voltage source for applying a select voltage to the gate of the first memory transistor via a first one of the word select lines, the select voltage having a polarity and magnitude relative to the body voltage sufficient to attract the hot electrons of the first memory transistor and change the threshold voltage thereof to a programmed state; and a voltage source for applying an unselect voltage to the gate of the second memory cell via a second one of the word select lines, the unselect voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons of the second memory transistor and deter change in the threshold voltage thereof.

Kindly delete paragraph [0019].